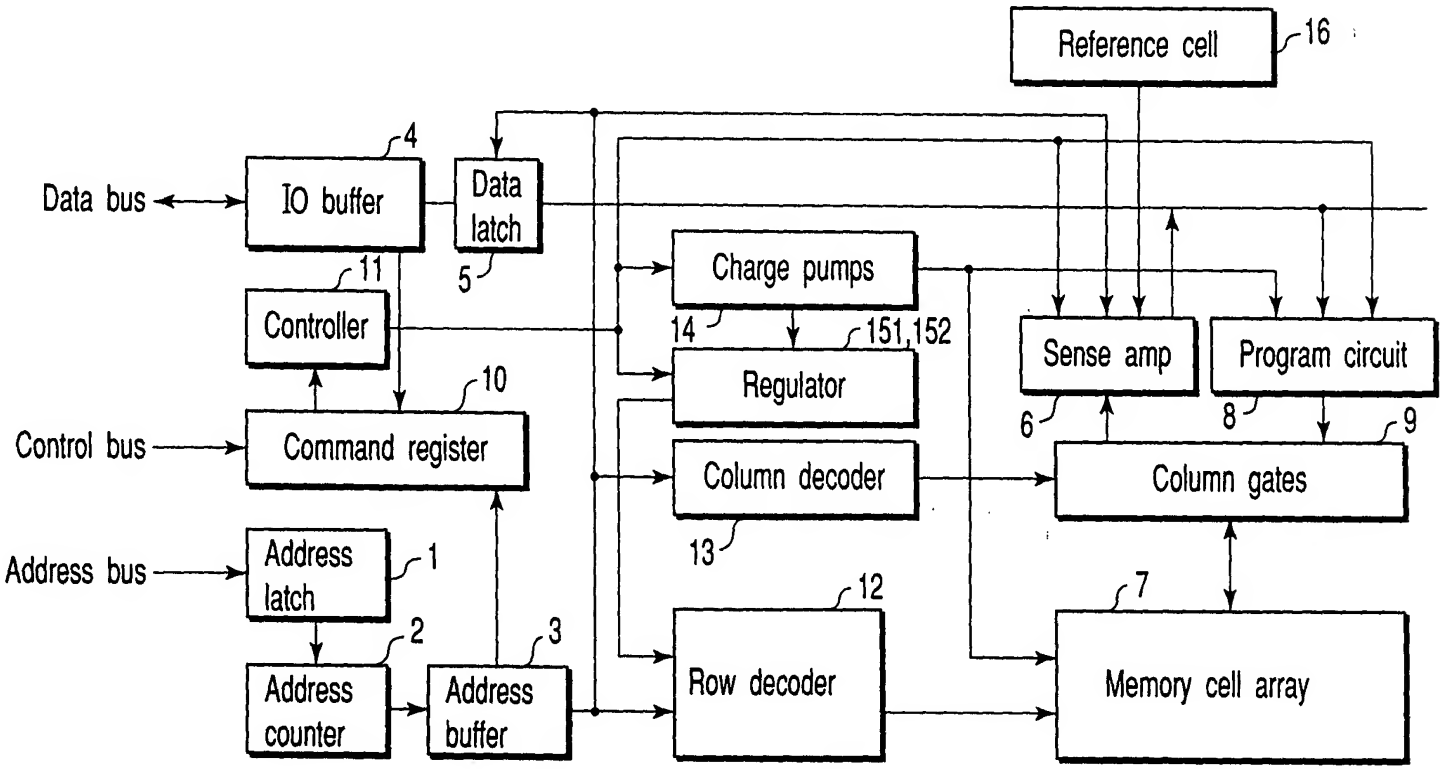

Reference cell
16
Data bus
IO buffer
4
Data latch
5
Charge pumps
14
151,152
Regulator
Sense amp
Program circuit
6
8
9
11
Controller
10
Control bus
Command register
Column decoder
13
Column gates
Address bus
Address latch
1
12
7
2
3
Address counter
Address buffer
Row decoder
Memory cell array

FIG. 1

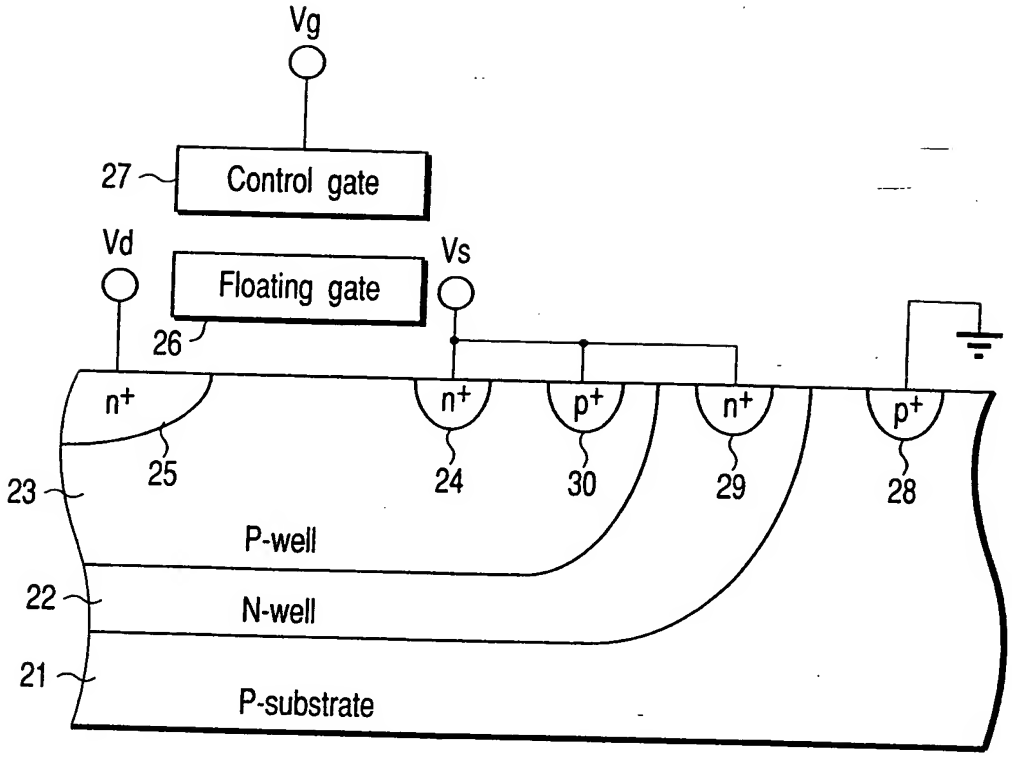

Vg
27
Control gate
Vd
Floating gate
Vs
26
n+
n+
p+
n+
p+
25
24
30
29
28
23
P-well
22
N-well
21
P-substrate

FIG. 2A

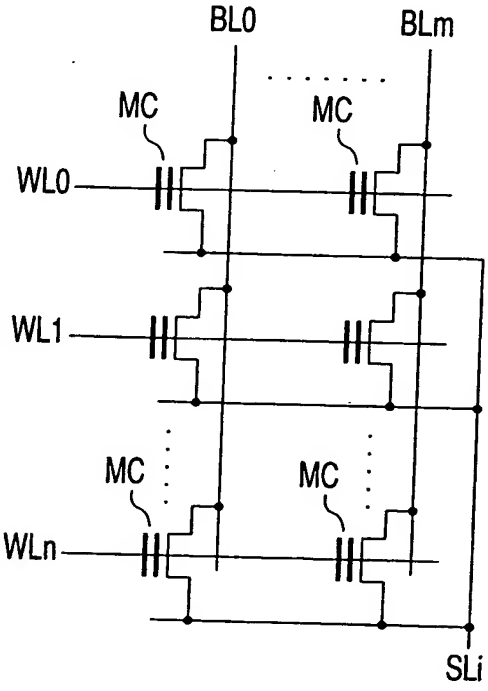

BL0
BLm
MC
MC
WL0
WL1
MC
MC
WLn
SLi

FIG. 2B

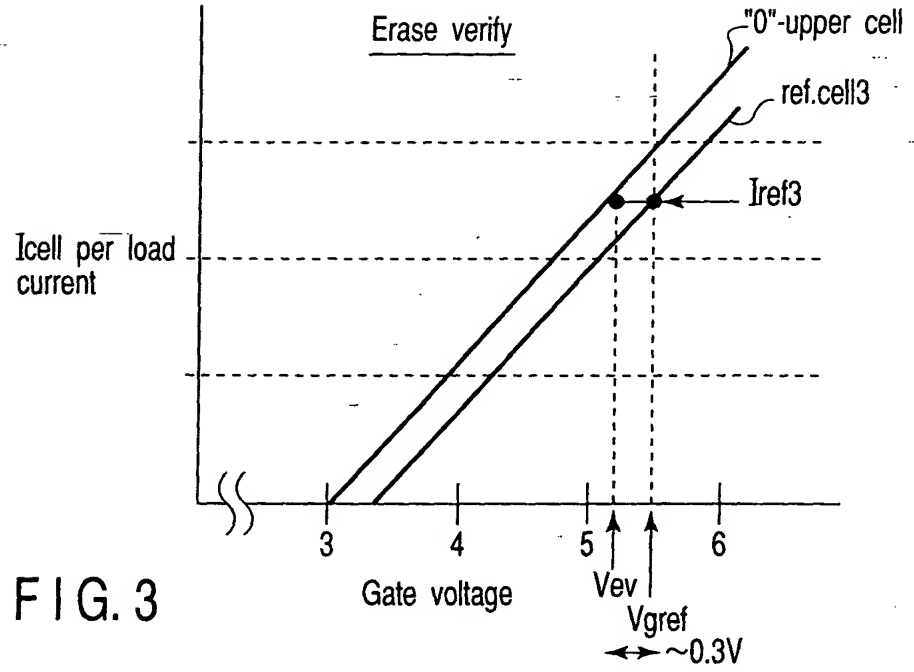

Erase verify
"0"-upper cell
ref.cell3
Iref3
Icell per load current
3
4
5
6
Vev
Vgref
~0.3V
Gate voltage

FIG. 3

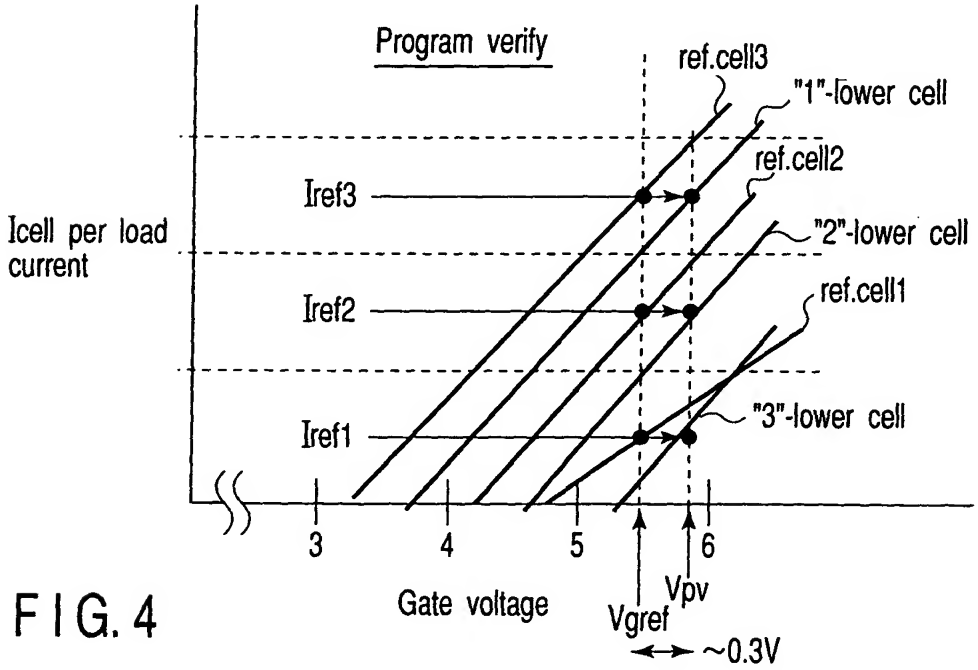
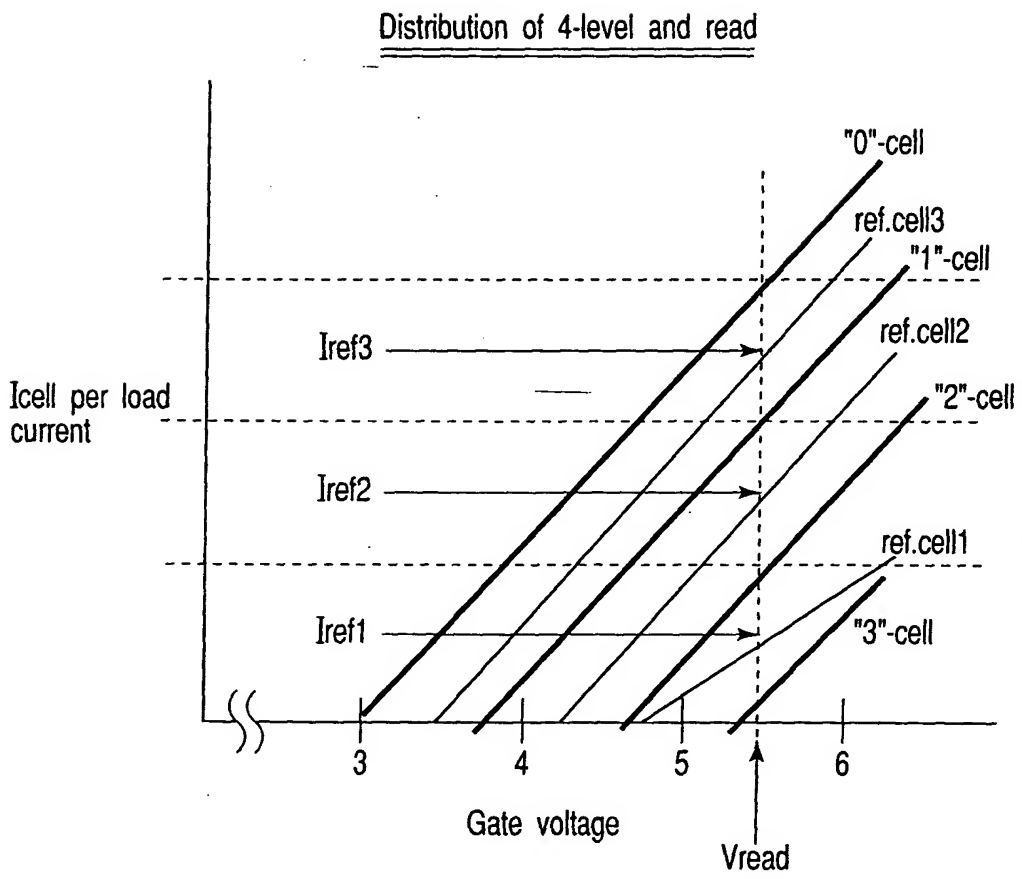

Program verify
ref.cell3
"1"-lower cell
ref.cell2
Iref3
Icell per load current
"2"-lower cell
ref.cell1
Iref2
"3"-lower cell
Iref1
3
4
5
6
Vpv
Vgref
~0.3V
Gate voltage

FIG. 4



During read : Vg = Vddr (memory cell, reference cell)
During verify :Vg = Vsw (memory cell)
Vg=Vswref (reference cell)

FIG. 5

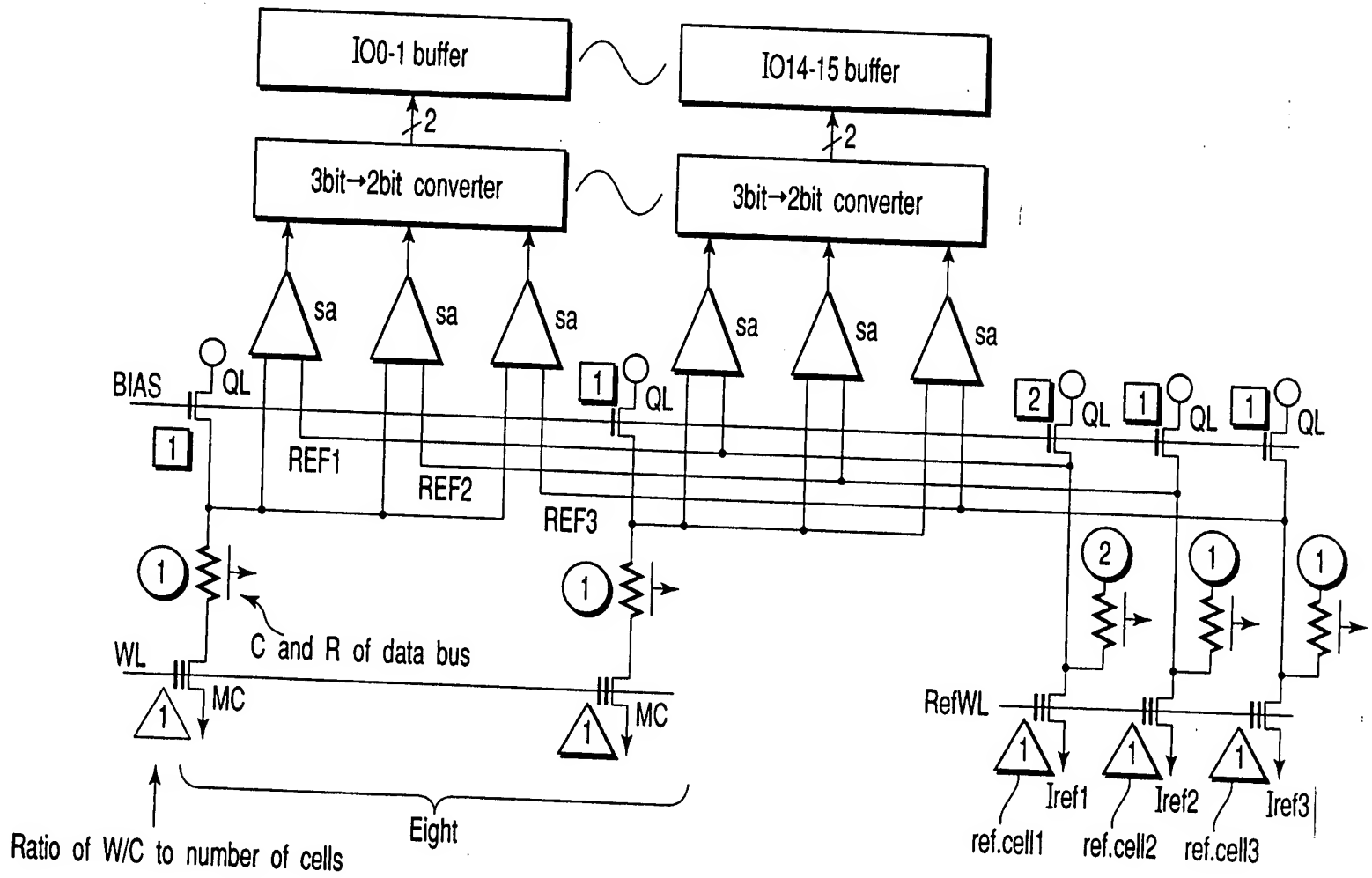

IO0-1 buffer
IO14-15 buffer
2
2
3bit→2bit converter
3bit→2bit converter
sa
sa
sa
sa
sa
sa
BIAS
QL
1
QL
2
QL
1
QL
1
QL
1
REF1
REF2
REF3
1
1
2
1
1
C and R of data bus
WL
MC
MC
RefWL
1
1
1
1
1
Iref1
Iref2
Iref3
ref.cell1
ref.cell2
ref.cell3
Eight
Ratio of W/C to number of cells

FIG. 6

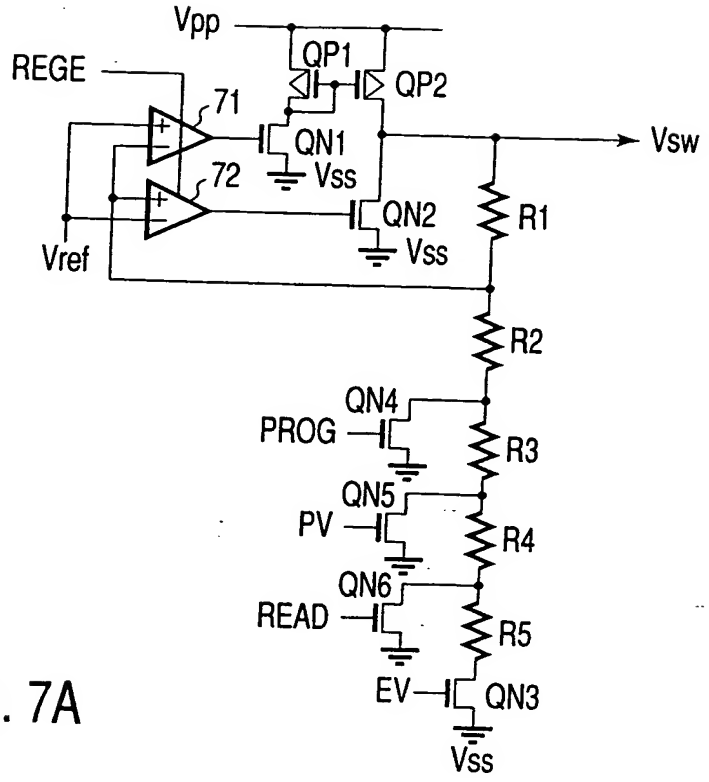

Vpp
REGE
QP1
QP2
71
QN1
Vsw
72
Vss
QN2
R1
Vref
Vss
R2
QN4
PROG
R3
QN5
PV
R4
QN6
READ
R5
EV
QN3
Vss

FIG. 7A

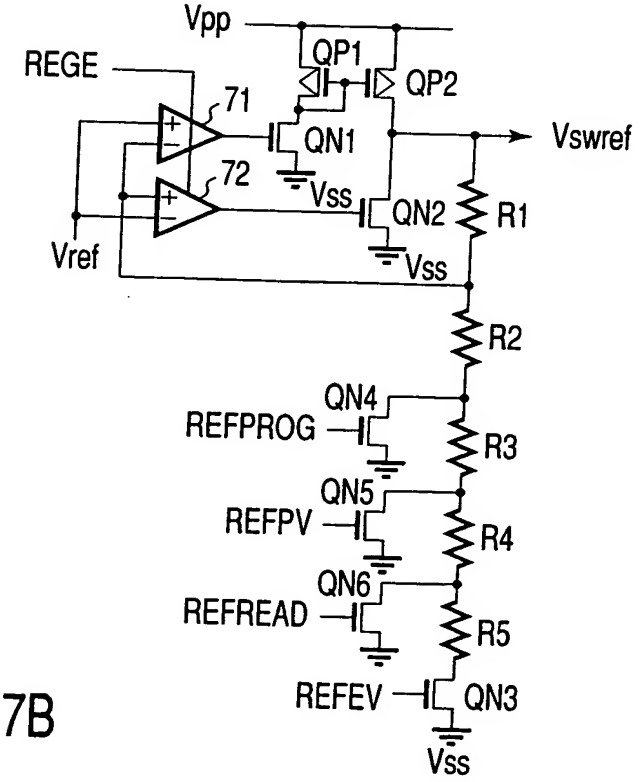

Vpp
REGE
QP1
QP2
71
QN1
Vswref
72
Vss
QN2
R1
Vref
Vss
R2
QN4
REFPROG
R3
QN5
REFPV
R4
QN6
REFREAD
R5
REFEV
QN3
Vss

FIG. 7B

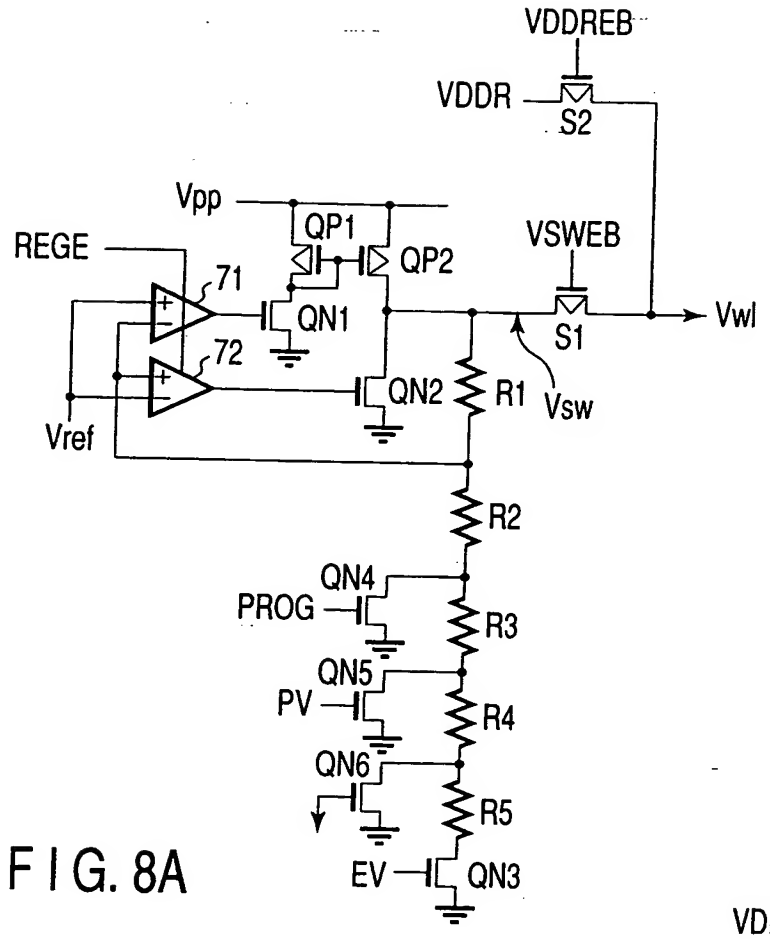

VDDREB
VDDR
S2
Vpp
QP1
QP2
REGE
71
VSWEB
QN1
Vwl
S1
72
QN2
R1
Vsw
Vref
R2
QN4
PROG
R3
QN5
PV
R4
QN6
R5
EV
QN3

FIG. 8A

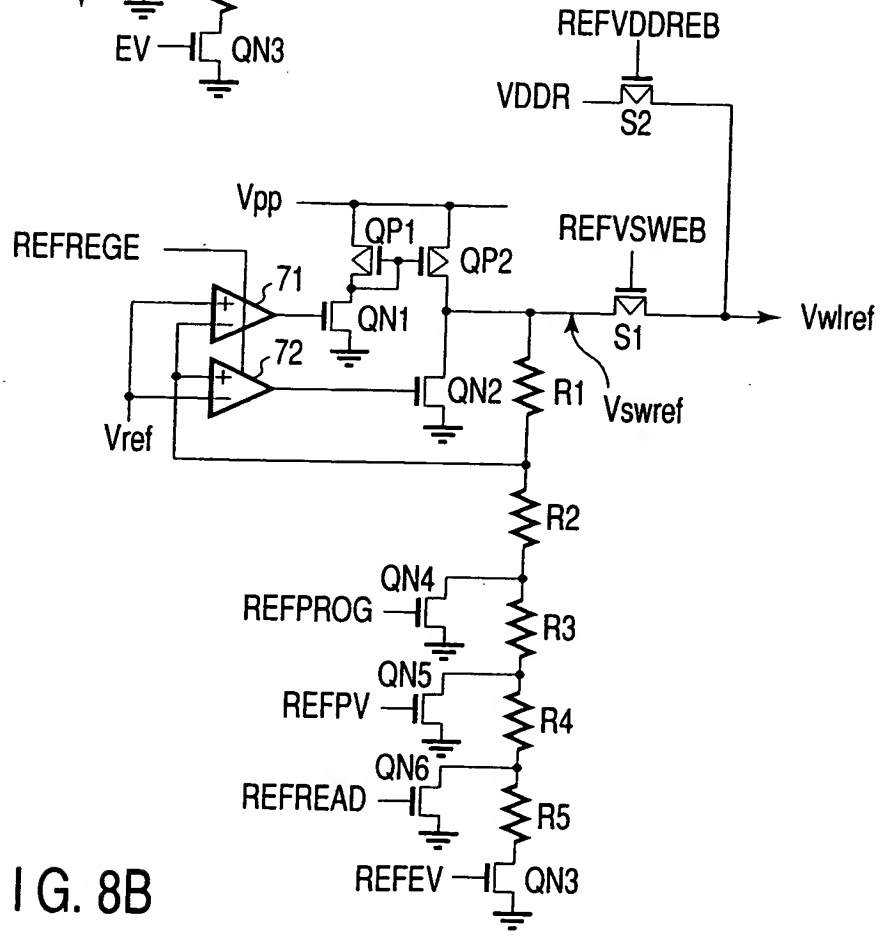
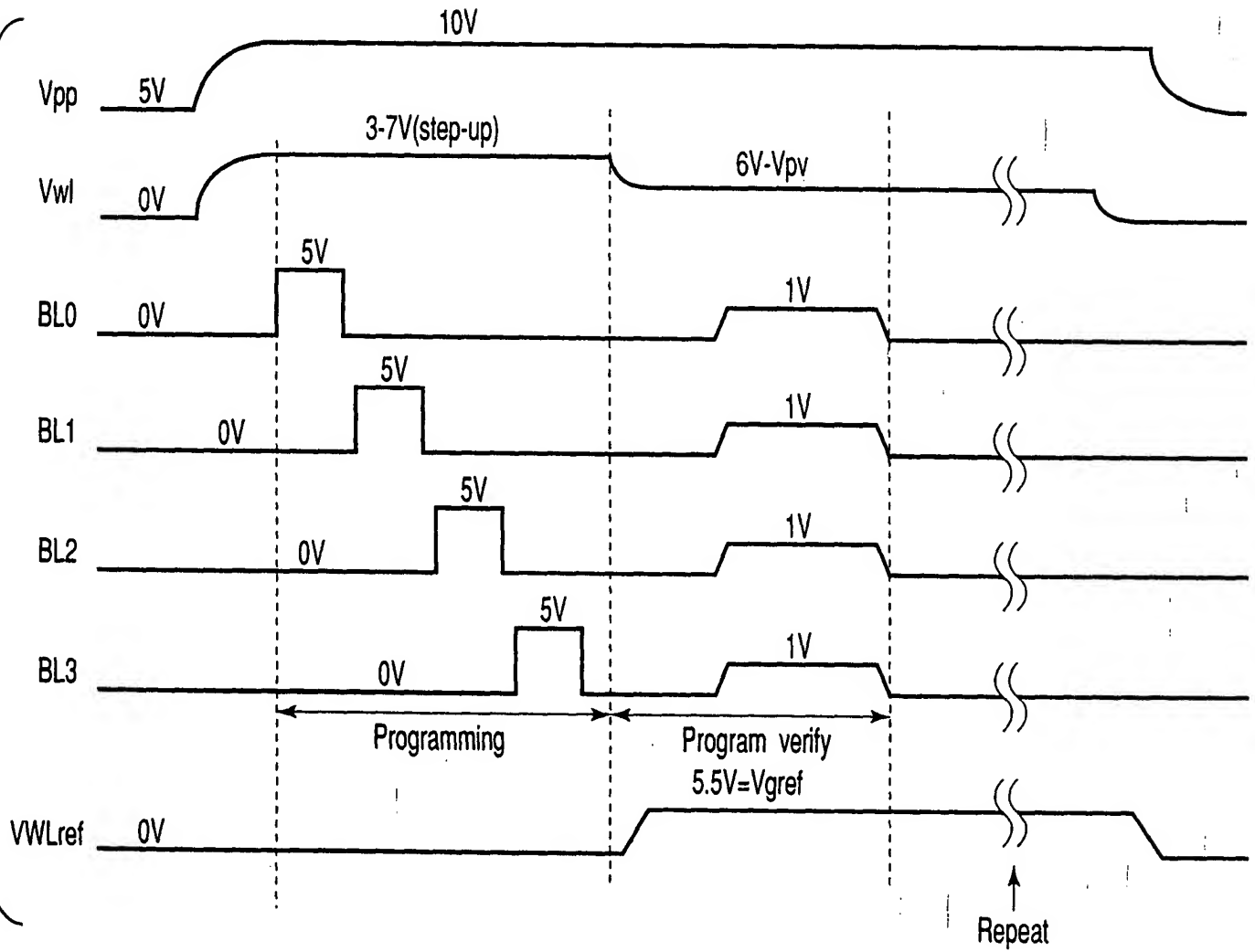

REFVDDREB
VDDR
S2
Vpp
QP1
QP2
REFREGE
71
REFVSWEB
QN1
Vwlref
S1
72
QN2
R1
Vswref
Vref
R2
QN4
REFPROG
R3
QN5
REFPV
R4
QN6
REFREAD
R5
REFEV
QN3

FIG. 8B

FIG. 9


10V
Vpp
5V
3-7V(step-up)
Vwl
0V
6V-Vpv
5V
BL0
0V
1V
5V
BL1
0V
1V
5V
BL2
0V
1V
5V
BL3
0V
1V
Programming
Program verify
5.5V=Vgref
VWLref
0V
Repeat

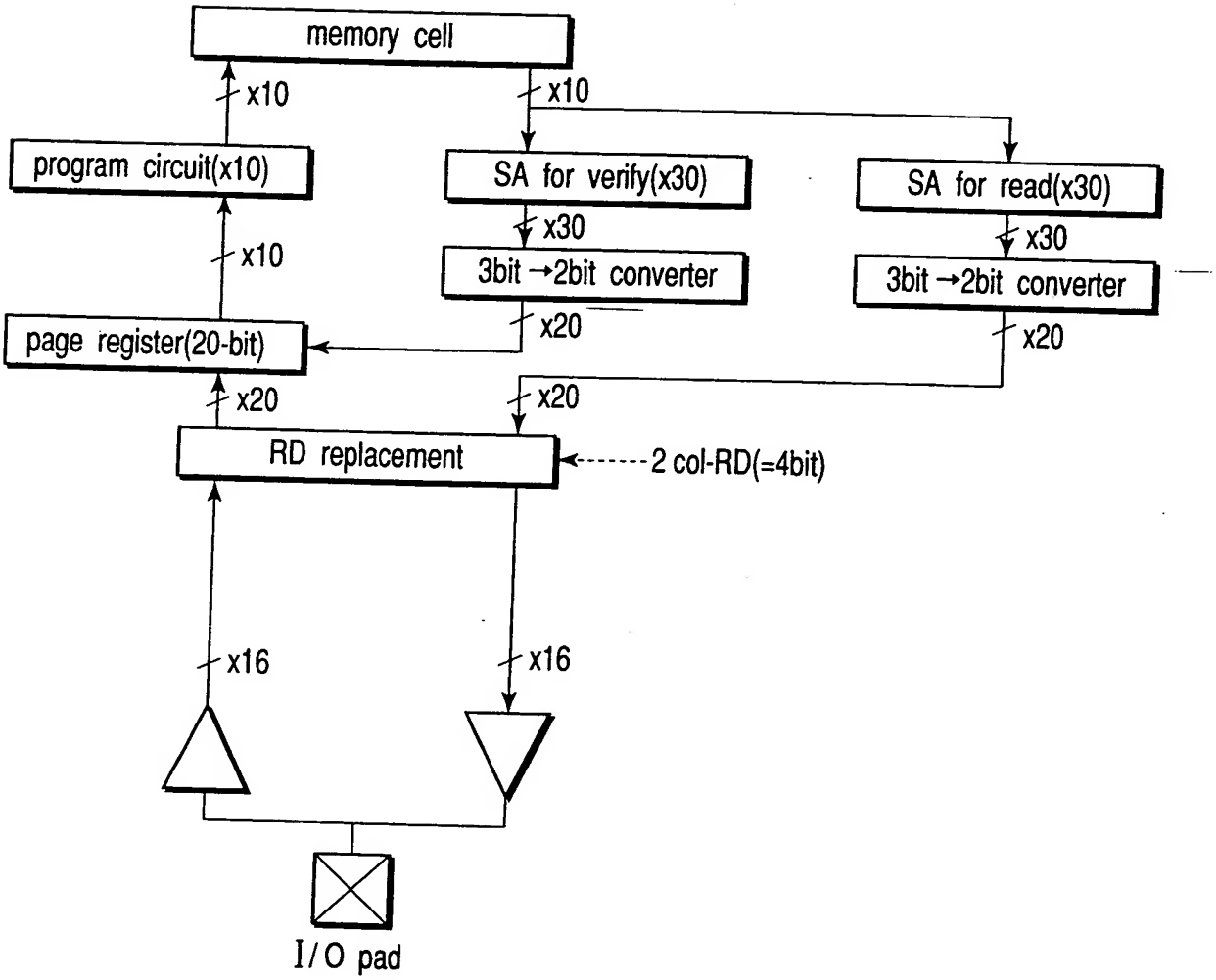

memory cell
x10
x10
program circuit(x10)
SA for verify(x30)
SA for read(x30)
x30
x30
x10
3bit →2bit converter
3bit →2bit converter
x20
x20
page register(20-bit)
x20
x20
RD replacement
2 col-RD(=4bit)
x16
x16
I/O pad

FIG. 10

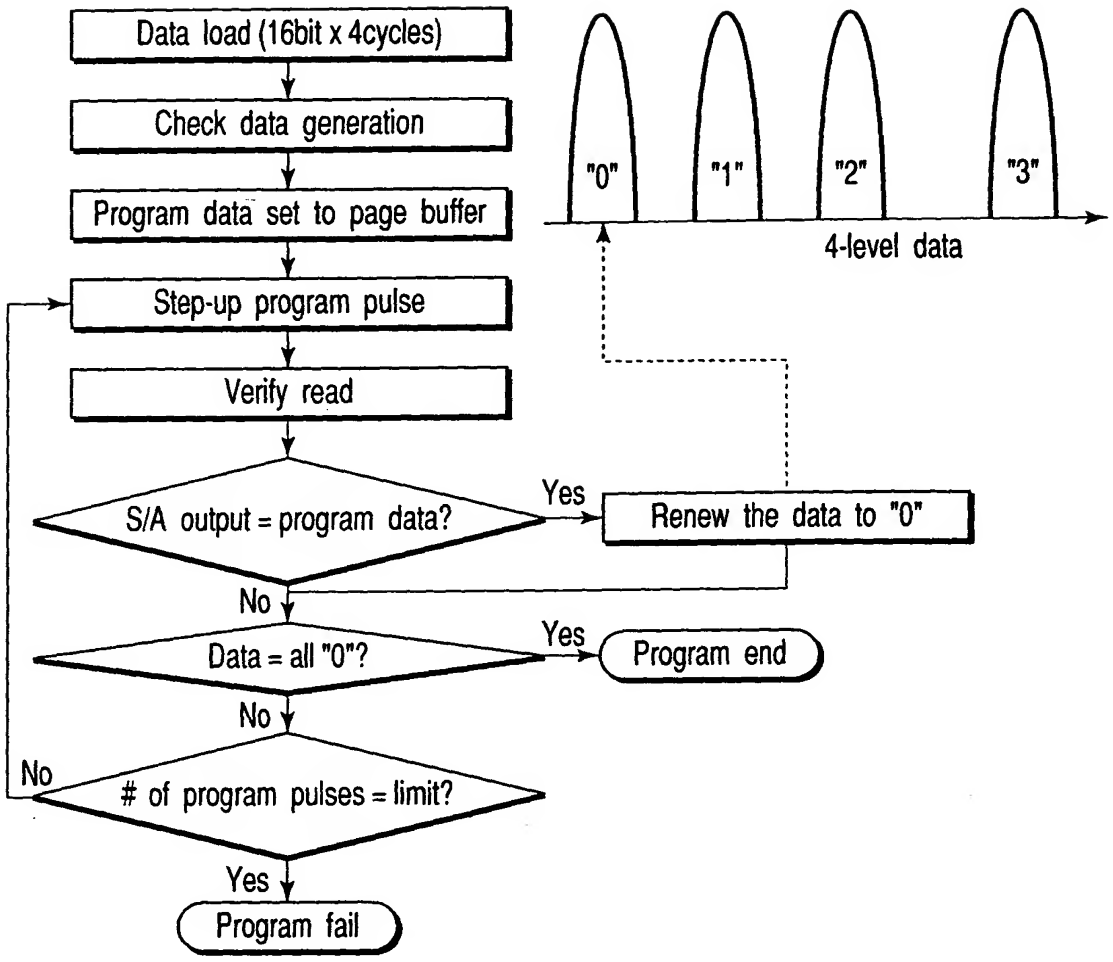

Data load (16bit x 4cycles)
Check data generation
Program data set to page buffer
Step-up program pulse
Verify read
S/A output = program data?
Yes
Renew the data to "0"
No
Data = all "0"?
Yes
Program end
No
# of program pulses = limit?
No
Yes
Program fail
"0"
"1"
"2"
"3"
4-level data

FIG. 11

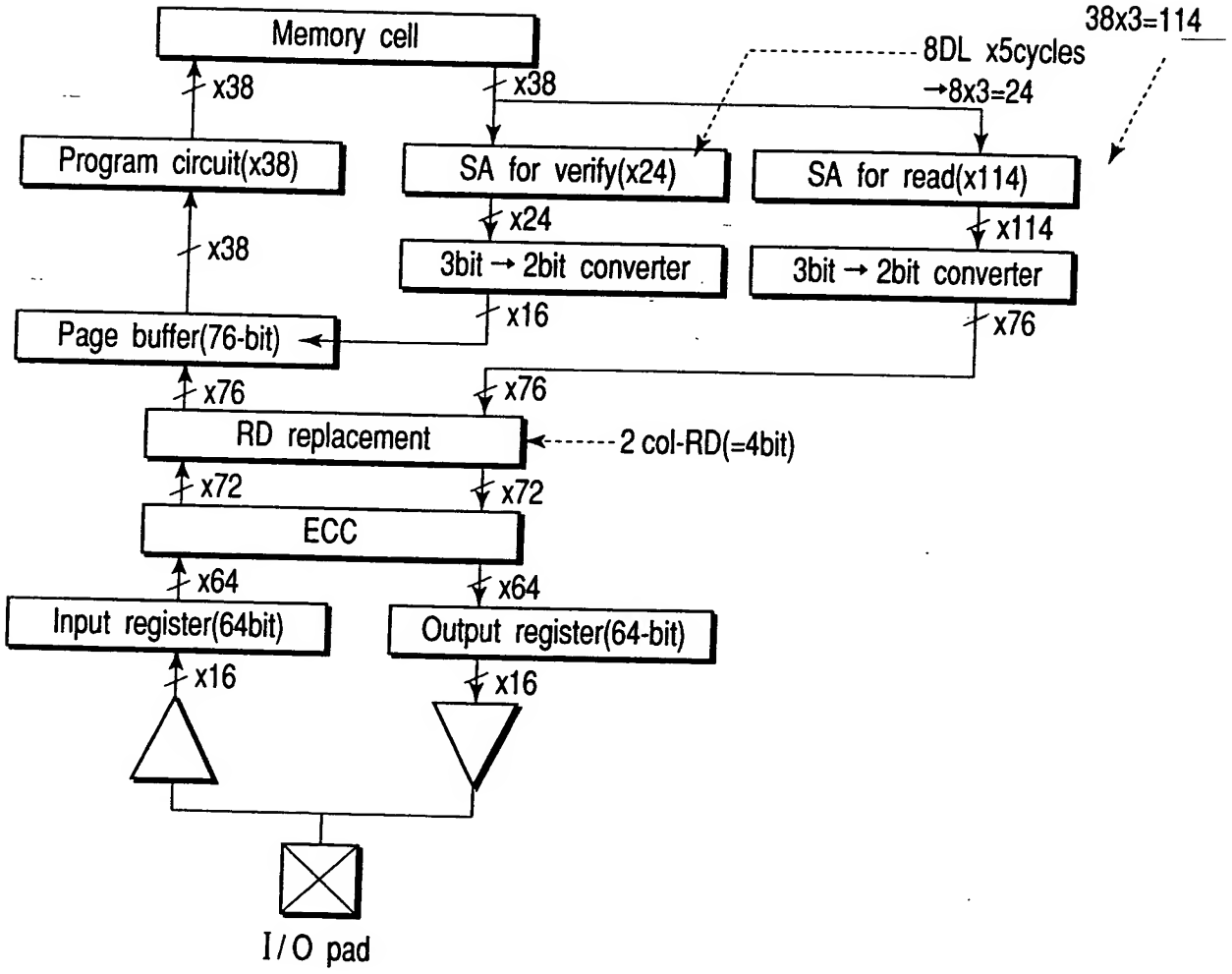

Memory cell
38x3=114
8DL x5cycles
→8x3=24
x38
x38
Program circuit(x38)
SA for verify(x24)
SA for read(x114)
x24
x114
x38
3bit → 2bit converter
3bit → 2bit converter
x16
x76
Page buffer(76-bit)
x76
x76
RD replacement
2 col-RD(=4bit)
x72
x72
ECC
x64
x64
Input register(64bit)
Output register(64-bit)
x16
x16
I/O pad

FIG. 12

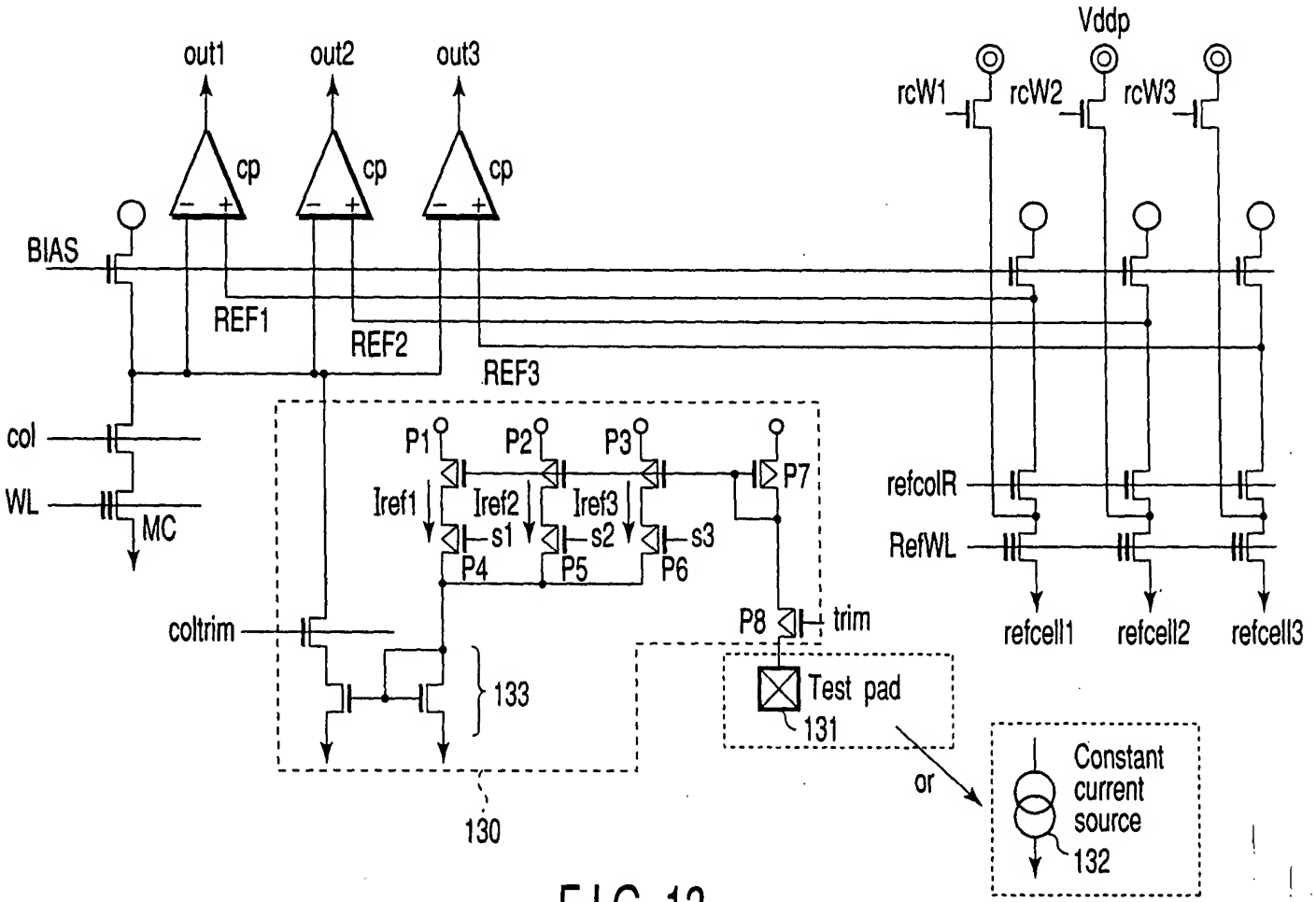

Vddp
out1
out2
out3
rcW1
rcW2
rcW3
cp
cp
cp
BIAS
REF1
REF2
REF3
col
WL
MC
P1
P2
P3
P7
Iref1
Iref2
Iref3
s1
s2
s3
P4
P5
P6
refcolR
RefWL
coltrim
P8
trim
refcell1
refcell2
refcell3
133
Test pad
131
or
Constant
current
source
132
130

FIG. 13

WL=0v
Col=0v
Coltrim=5v
Trim=0v
Vddp=5v

	s1	s2	s3	refWL	refcolR	rcw1	rcw2	rcw3	out1	out2	out3
Step1	Erase reference cells										
Step2	0v	5v	5v	5v	5v	0v	0v	0v	out1:L→step3/H→step4		
Step3	0v	5v	5v	9v	0v	9v	0v	0v	→step2		
Step4	5v	0v	5v	5v	5v	0v	0v	0v	out2:L→step5/H→step6		
Step5	5v	0v	5v	9v	0v	0v	9v	0v	→step4		
Step6	5v	5v	0v	5v	5v	0v	0v	0v	out3:L→step7/H→step8		
Step7	5v	5v	0v	9v	0v	0v	0v	9v	→>step8		
Step8	Trim end										

FIG. 14

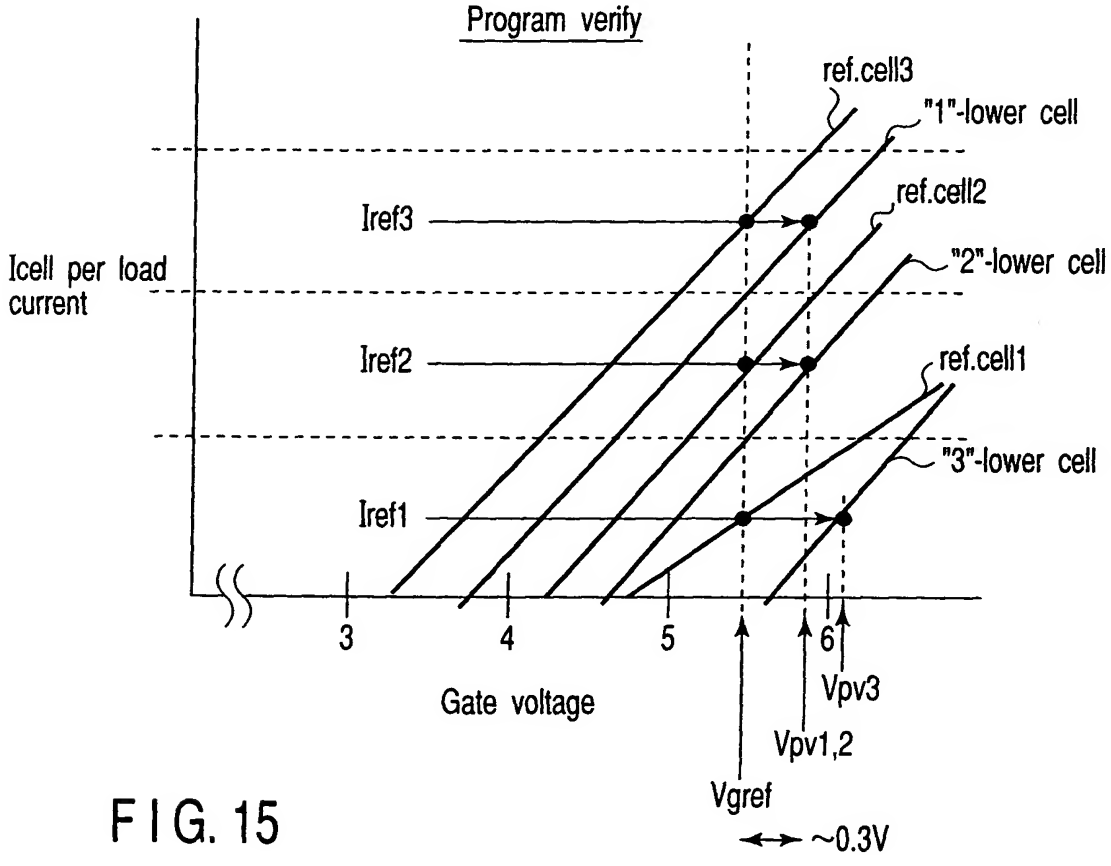


FIG. 15

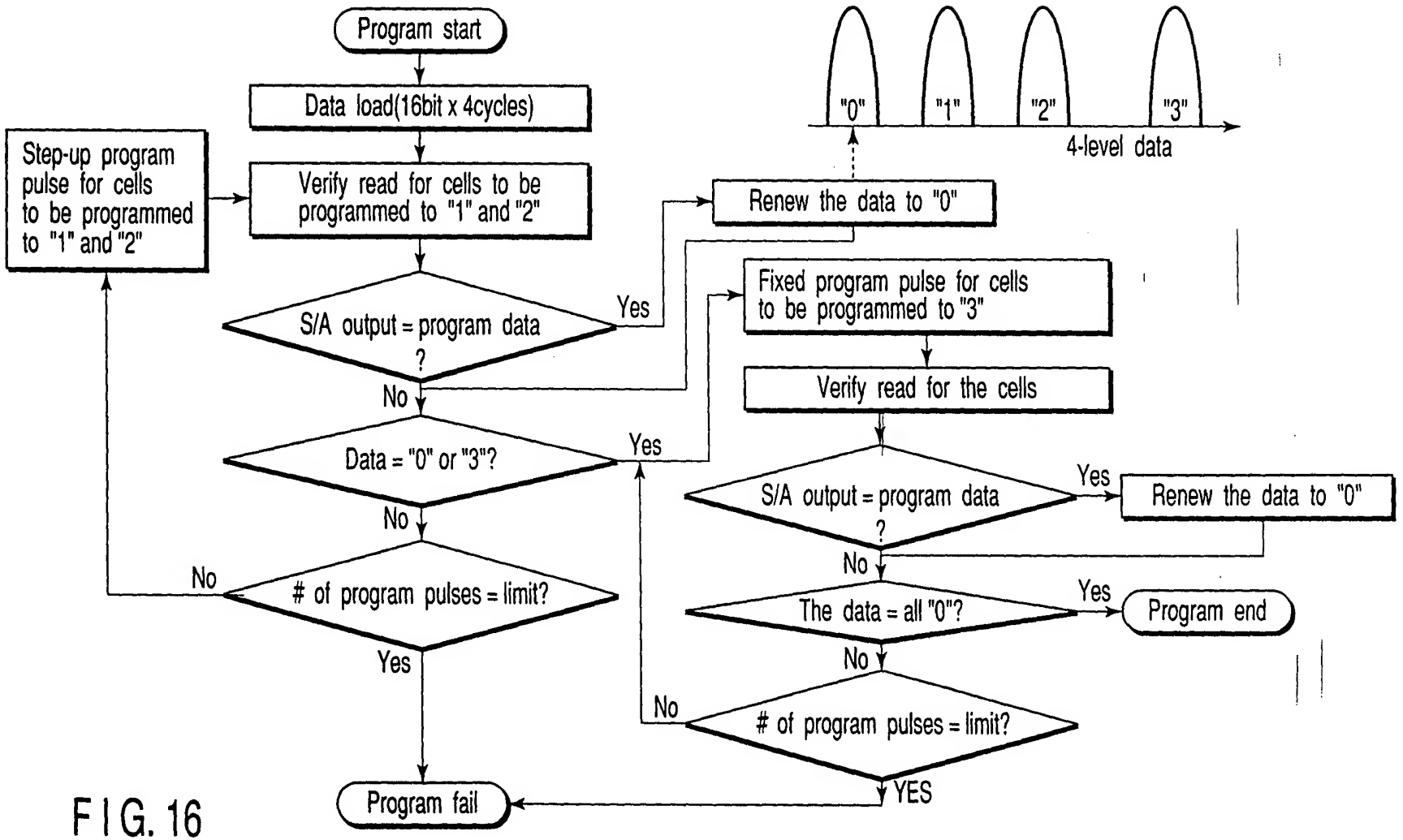

Program start
Data load(16bit x 4cycles)
Step-up program pulse for cells to be programmed to "1" and "2"
Verify read for cells to be programmed to "1" and "2"
S/A output = program data ?
Yes
No
Renew the data to "0"
"0"
"1"
"2"
"3"
4-level data
Fixed program pulse for cells to be programmed to "3"
Verify read for the cells
Data = "0" or "3"?
Yes
No
S/A output = program data ?
Yes
Renew the data to "0"
No
# of program pulses = limit?
No
Yes
The data = all "0"?
Yes
Program end
No
No
# of program pulses = limit?
YES
Program fail

FIG. 16

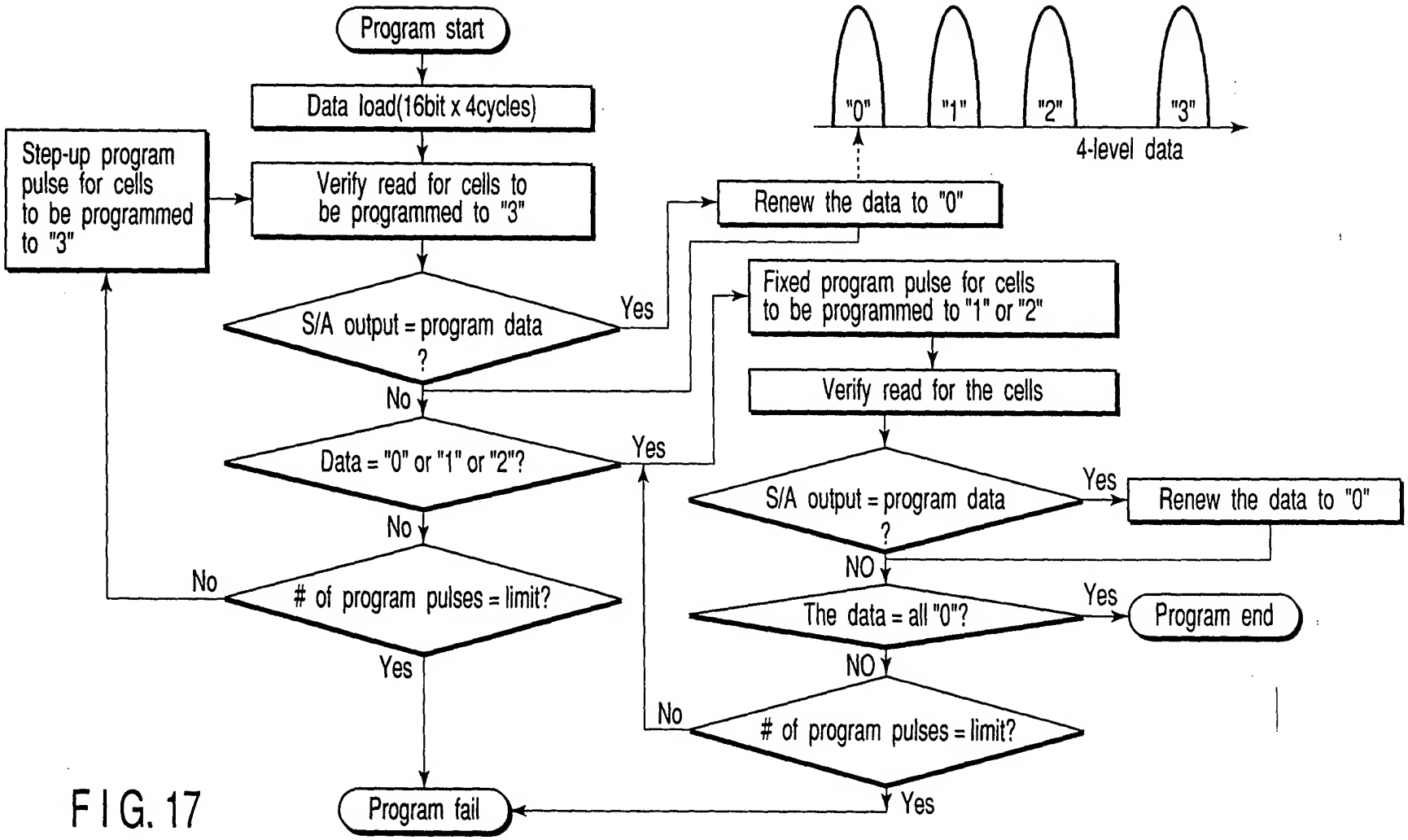
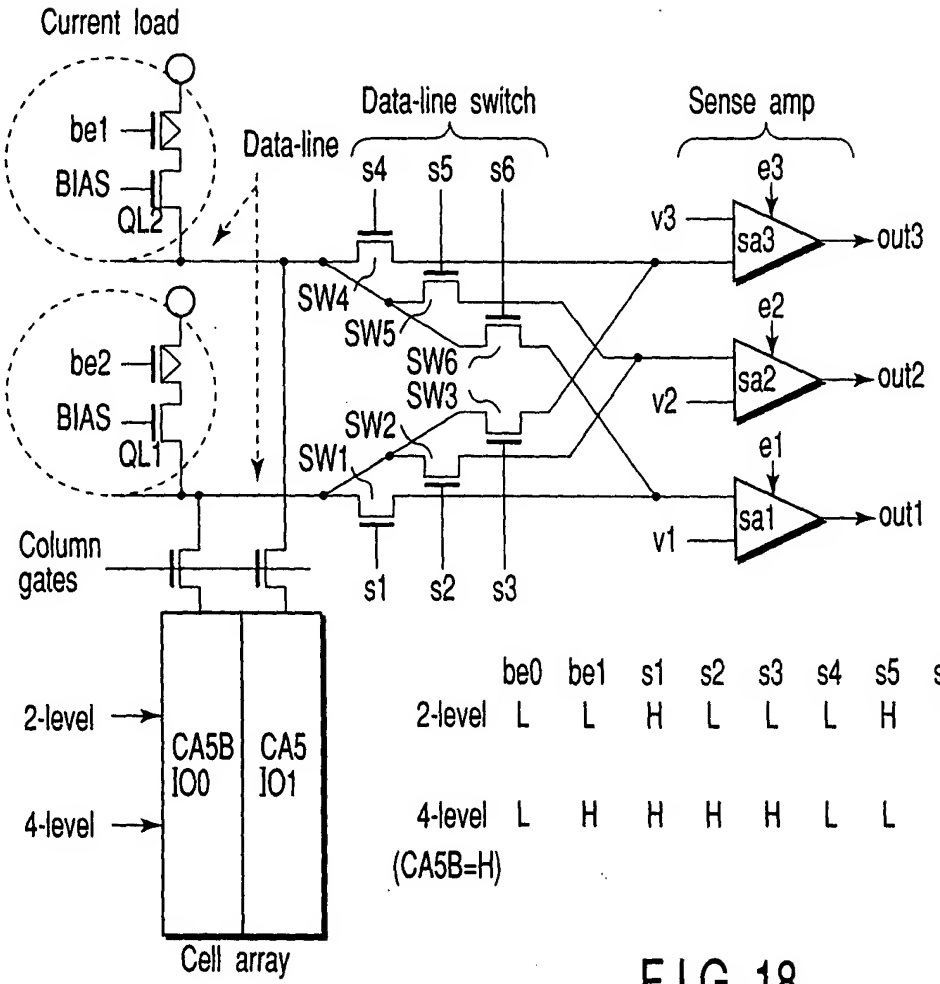

Program start
Data load(16bit x 4cycles)
Step-up program pulse for cells to be programmed to "3"
Verify read for cells to be programmed to "3"
S/A output = program data ?
Yes
No
Renew the data to "0"
"0"
"1"
"2"
"3"
4-level data
Fixed program pulse for cells to be programmed to "1" or "2"
Verify read for the cells
Data = "0" or "1" or "2"?
Yes
No
S/A output = program data ?
Yes
Renew the data to "0"
NO
No
# of program pulses = limit?
The data = all "0"?
Yes
Program end
NO
No
# of program pulses = limit?
Yes
Yes
Program fail

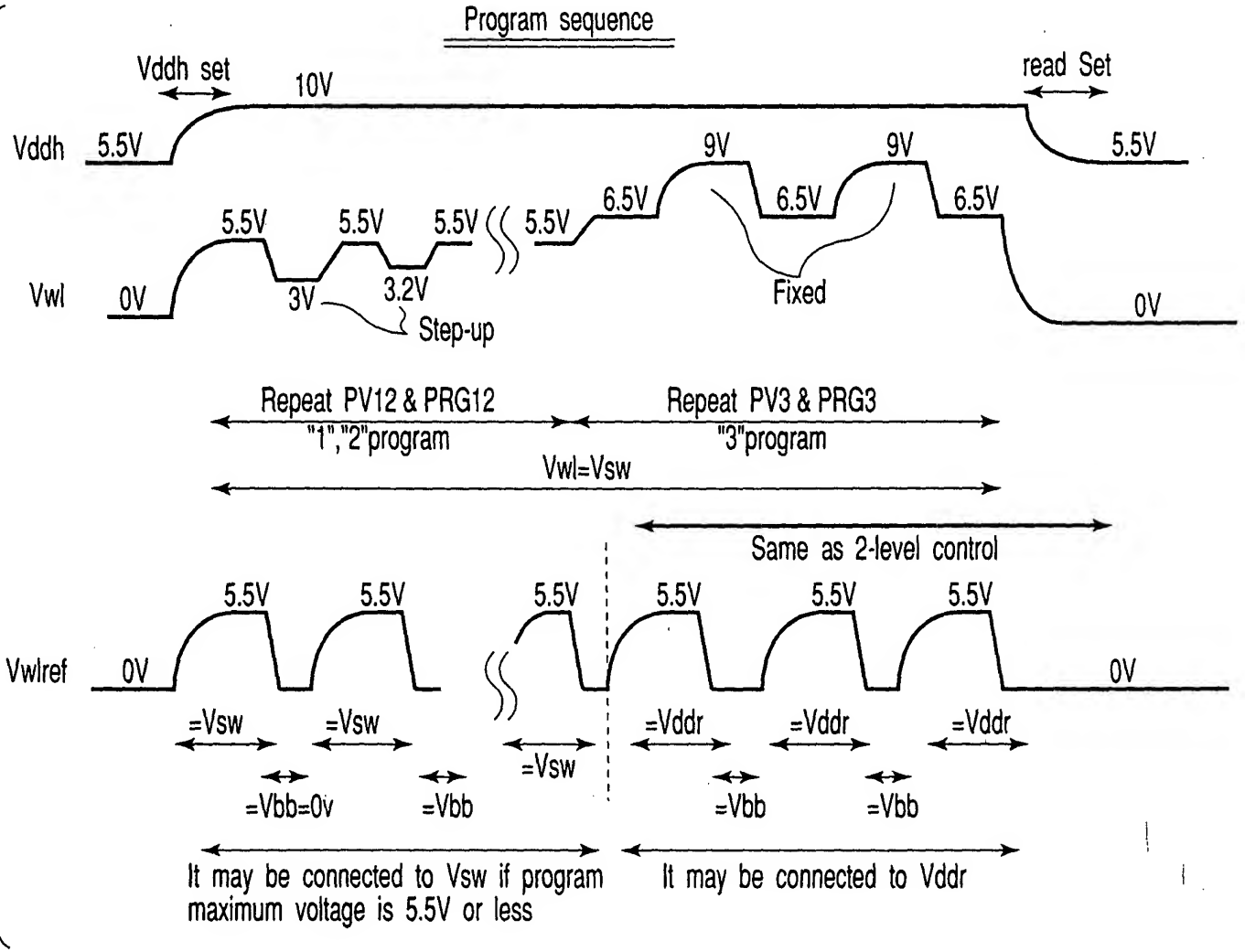
FIG. 17



	be0	be1	s1	s2	s3	s4	s5	s6	v1	v2	v3	e1	e2	e3	out1	out2	out3
2-level	L	L	H	L	L	L	H	L	REF2-level			H	H	L	IO0	IO1	NA
4-level (CA5B=H)	L	H	H	H	H	L	L	L	REF1,2,3			H	H	H	to-"3-to-2-conv."		

FIG. 18

FIG. 19


Program sequence
Vddh set
10V
read Set
Vddh
5.5V
5.5V
9V
9V
6.5V
6.5V
6.5V
Vwl
0V
5.5V
5.5V
5.5V
3V
3.2V
Step-up
Fixed
0V
Repeat PV12 & PRG12
"1","2"program
Repeat PV3 & PRG3
"3"program
Vwl=Vsw
Same as 2-level control
Vwlref
0V
5.5V
5.5V
5.5V
5.5V
5.5V
5.5V
0V
=Vsw
=Vsw
=Vsw
=Vddr
=Vddr
=Vddr
=Vbb=0v
=Vbb
=Vbb
=Vbb
It may be connected to Vsw if program maximum voltage is 5.5V or less
It may be connected to Vddr

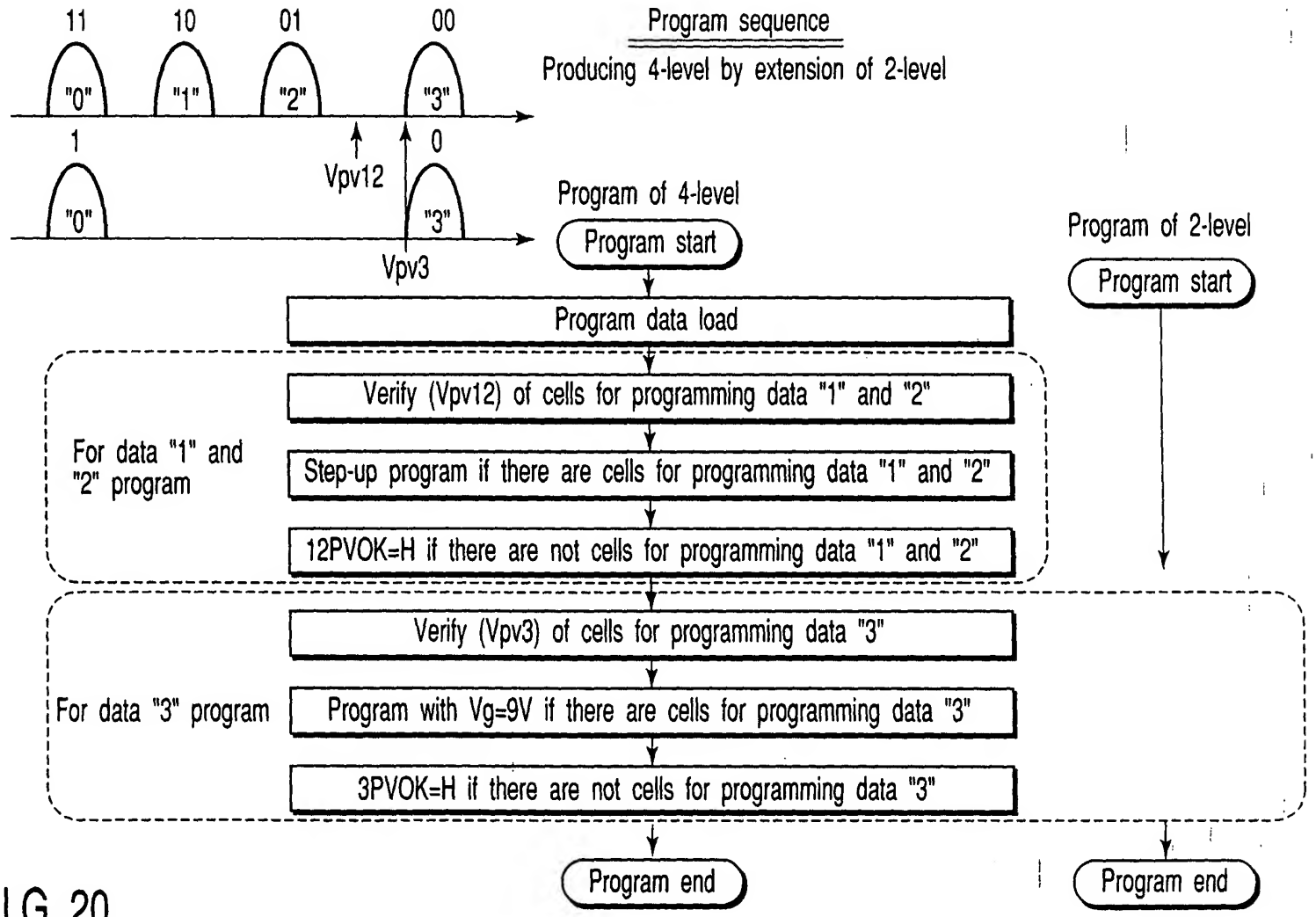

11
10
01
00
"0"
"1"
"2"
"3"
Program sequence
Producing 4-level by extension of 2-level
1
0
Vpv12
"0"
"3"
Vpv3
Program of 4-level
Program start
Program data load
Verify (Vpv12) of cells for programming data "1" and "2"
For data "1" and "2" program
Step-up program if there are cells for programming data "1" and "2"
12PVOK=H if there are not cells for programming data "1" and "2"
Verify (Vpv3) of cells for programming data "3"
For data "3" program
Program with Vg=9V if there are cells for programming data "3"
3PVOK=H if there are not cells for programming data "3"
Program end
Program of 2-level
Program start
Program end

FIG. 20

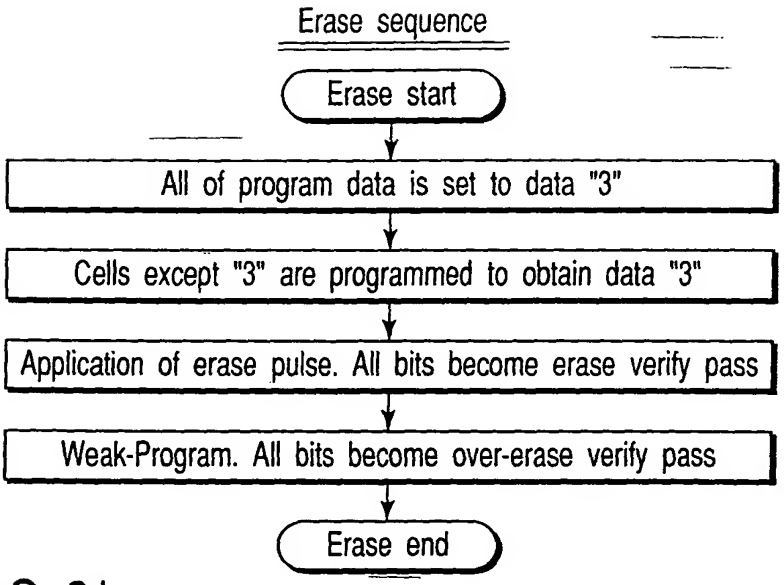
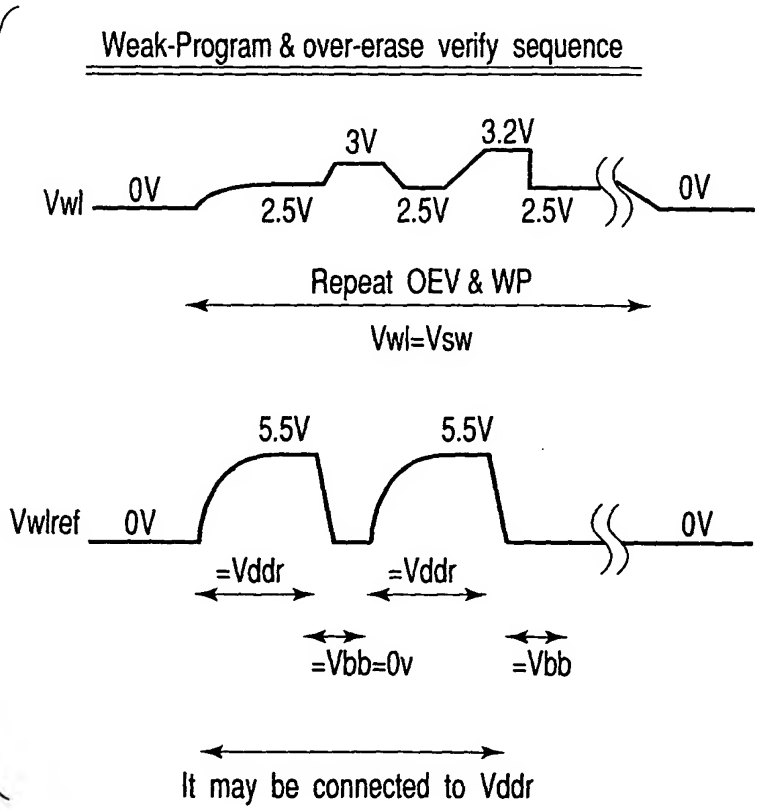

Erase sequence
Erase start
All of program data is set to data "3"
Cells except "3" are programmed to obtain data "3"
Application of erase pulse. All bits become erase verify pass
Weak-Program. All bits become over-erase verify pass
Erase end

FIG. 21

FIG. 22


Weak-Program & over-erase verify sequence
Vwl
0V
3V
3.2V
2.5V
2.5V
2.5V
0V
Repeat OEV & WP
Vwl=Vsw
Vwlref
0V
5.5V
5.5V
0V
=Vddr
=Vddr
=Vbb=0v
=Vbb
It may be connected to Vddr

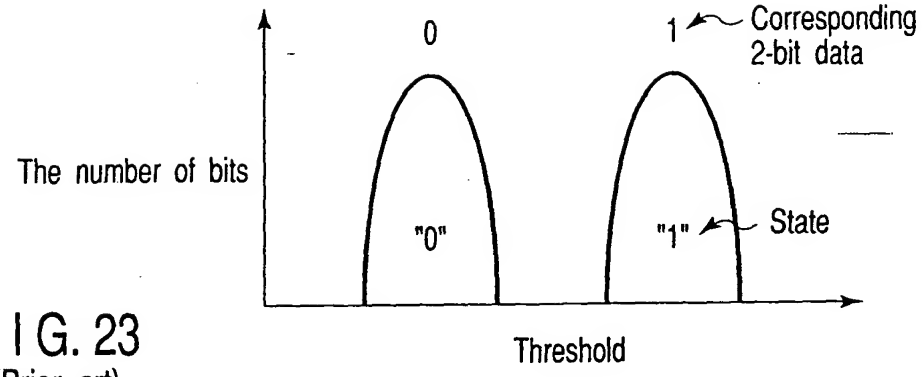


FIG. 23
(Prior art)

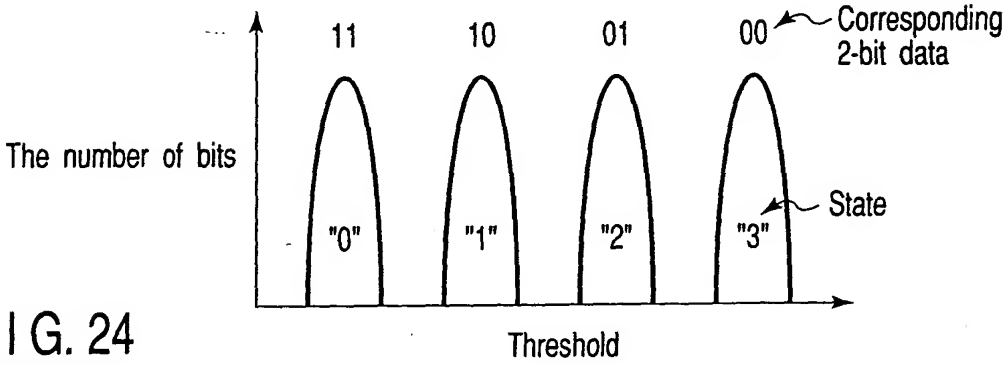


FIG. 24
(Prior art)

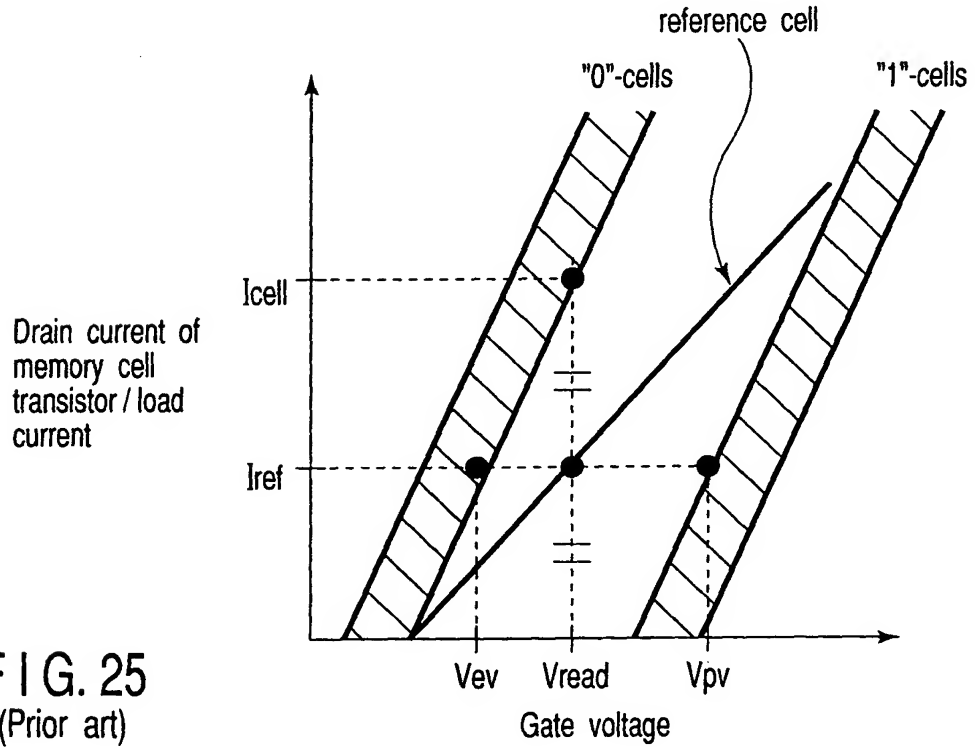


FIG. 25
(Prior art)

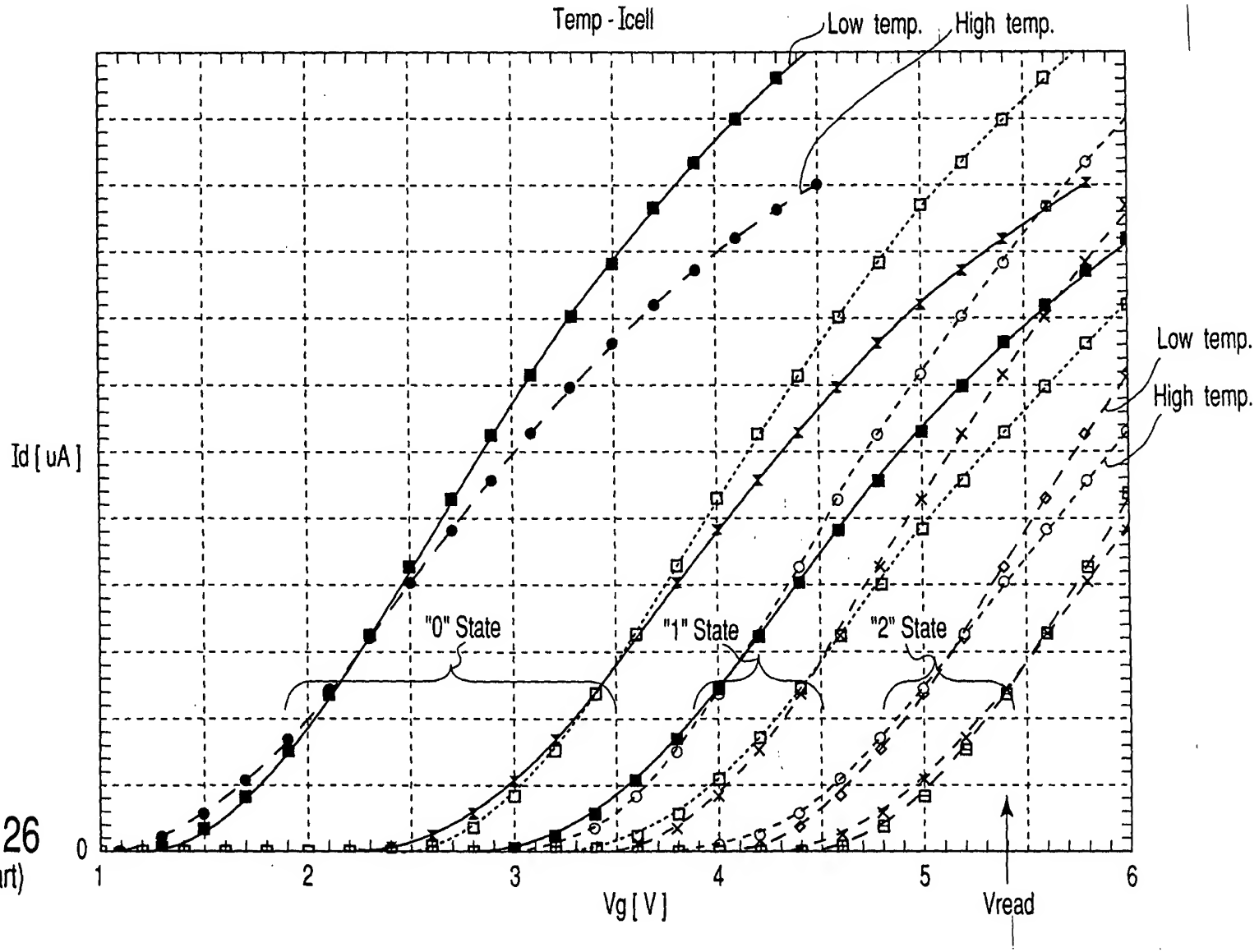


FIG. 26
(Prior art)